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WHAT IS CLAIMED IS:

1. A process for fabricating an integrated circuit structure comprising:

forming a first contact region selected from the group consisting of a source contact region and a drain contact region of a semiconductor device in a semiconductor substrate;

forming a multilayer stack comprising at least three layers of material over the first contact region, wherein the second layer is interposed between the first and the third layers and wherein the first layer is proximate the first contact region;

forming a window in the at least three layers of material, wherein the window does not extend into the first contact region;

forming semiconductor material along at least one vertical wall of the window, wherein the semiconductor material comprises vertically-oriented first, second and third doped regions, and wherein the first doped region is adjacent the first layer and further is in electrical contact with the first contact region, and wherein a second doped region of the semiconductor material is adjacent the second layer, and wherein the third doped region is adjacent the third layer;

forming insulating material on the inwardly-facing surface of at least the first and the third doped regions in the window;

removing the second layer, thereby exposing at least a portion of the second doped region; and

forming a gate dielectric layer in contact with the second doped region.

forming a gate in contact with said gate dielectric layer.

2. The process of claim 1 wherein the second layer is removed by etching in an etchant, characterized by a first layer etch rate, a second layer etch rate, and a third layer etch rate, wherein the second layer etch rate is at least ten times faster than one of the first layer etch rate and the third layer etch rate.

3. The process of claim 1 wherein the material of the first layer and the third layer comprises an electrically insulating material.

4. The process of claim 3 wherein the electrically insulating material of at least one of the first and the third layers is doped silicon dioxide for doping, respectively, the first doped region and the third doped region, wherein the process further comprises

doping at least one of the first and the third doped regions of the semiconductor material by diffusing dopant from the adjacent first layer or the adjacent third layer.

5. The process of claim 1 wherein the semiconductor material is doped in situ, and wherein the material of at least one of the first layer and the third layer is doped silicon dioxide for doping the first doped region and the third doped region, respectively, and wherein the process further comprises counterdoping at least one of the first and the third doped regions of the semiconductor material by diffusing dopant from the adjacent first layer or the adjacent third layer.

6. The process of claim 1 wherein the semiconductor material comprises crystalline semiconductor material and is selected from the group consisting of silicon, silicon germanium, and silicon-germanium-carbon.

7. The process of claim 1 further comprising forming a second contact region selected from the group consisting of a source contact region and a drain contact region overlying the third doped region, wherein one of the first and second contact regions is a source contact region and the other is a drain contact region.

8. The process of claim 1 wherein the step of forming the semiconductor material further comprises:

forming polycrystalline silicon along at least one vertical wall region of the window; and

melting the polycrystalline silicon to form single-crystalline silicon, wherein the material of the first and the third layers is doped insulating material, and wherein during the step of melting the polycrystalline silicon, dopants in the first layer diffuse into the adjacent region of the semiconductor material to form the first doped region, and dopants in the third layer diffuse into the adjacent region of the semiconductor material to form the third doped region.

9. The process of claim 1 further comprising forming an insulating layer over the first layer of material, or over the second layer of material, or over both the first and the second layers of material.

10. The process of claim 9 wherein the insulating layer comprises an etch stop layer.

11. The process of claim 10 wherein a first layer of insulating material is formed over the first layer and a second layer of insulating material is formed over the second layer, and wherein the first and the second layers of insulating material comprise diffusion barriers, and wherein the material of the first layer is doped silicon dioxide that serves as a dopant source for the first doped region and the material of the third layer is doped silicon dioxide that serves as the dopant source for the third doped region, and wherein the process further comprises doping the first doped region of the semiconductor material by diffusing dopant from the first layer and doping the third doped region of the semiconductor material by diffusing dopant from the third layer, and wherein the diffusion barrier presented by the first layer of insulating material effectively prevents the upward diffusion of dopants from the first layer, and wherein the diffusion barrier presented by the second layer of insulating material effectively prevents the upward diffusion of dopants from the third layer.

12. The process of claim 1 wherein the window has a generally circular or ellipsoidal cross section in a plane parallel to the top surface of the semiconductor substrate, and wherein the semiconductor material is formed adjacent the inner wall of the window, and wherein the first, the second and the third doped regions comprise stacked annular rings of the semiconductor material adjacent the inner wall of the window.

13. The process of claim 1 wherein the window has a generally rectangular cross section along a plane parallel to the top surface of the semiconductor substrate, and wherein two insulated regions of semiconductor material are formed adjacent opposing inner wall regions of the window, and wherein the first, the second and the third doped regions are formed in each one of the two regions of semiconductor material, such that two parallel vertical silicon-on-insulator transistors are formed.

14. The process of claim 1 wherein the step of forming insulating material in the window further comprises forming an insulating plug in the open volume of the window.

15. The process of claim 1 further comprising forming insulating material on the inside surface of the first and the third doped regions and forming conductive material on the inside surface of the second doped region.

16. The process of claim 15 wherein the conductive material is connected to ground.

17. The process of claim 15 further comprising:

forming insulating material on the inside surface of the first, second and third doped regions, wherein the insulating material is formed with a greater thickness on the inside surface of the first and the third doped regions due to the dopant concentration in the first and the third doped regions relative to the dopant concentration in the second doped region;

removing the insulating material on the inside surface of the second doped region such that insulating material remains on the inside surface of the first and the second doped regions; and

forming conductive material in electrical contact with the inside surface of the second doped region and electrically separated from the first and the third doped regions by the insulating material.

18. A process for fabricating a vertical silicon-on-insulator MOSFET comprising:

forming a first contact region selected from the group consisting of a source contact region and a drain contact region of a semiconductor device in a semiconductor substrate;

forming a multilayer stack comprising at least three layers of material over the first contact region, wherein the second layer is interposed between the first and the third layers, and wherein the first layer is proximate the first contact region;

forming a window in the at least three layers of material, wherein the window does not extend into the first contact region;

forming semiconductor material along at least one vertical wall region of the window, wherein the semiconductor or material comprises a first, a second and a third doped region, and wherein the first doped region is adjacent the first layer and is doped a first conductivity type and further is in electrical contact with the first contact region, and wherein the second doped region is adjacent the second layer and is doped a second conductivity type, and wherein the third doped region is adjacent the third layer and is doped the first conductivity type;

forming a first insulating surface adjacent the first doped region and extending toward the center of the window;

forming a second insulating surface adjacent the third doped region and extending toward the center of the window;

forming a conductive plug in the remaining open volume of the window, wherein a portion of the plug is in electrical contact with the second doped region on the surface of the second doped region facing the center of the window;

removing the second layer, thereby exposing at least a portion of the second doped region;

forming a gate dielectric layer in contact with the second doped region; and

forming a gate in contact with the gate dielectric layer.

19. The process of claim 18 wherein the second layer is removed by etching in an etchant, characterized by a first layer etch rate, a second layer etch rate, and a third layer etch rate, wherein the second layer etch rate is at least ten times faster than one of the first layer etch rate and the third layer etch rate.

20. The process of claim 18 wherein the material of the first, second and the third layer comprises doped insulating material, and wherein the process further comprises doping at least one of the first and the third doped regions by diffusing dopant from the first layer into the third doped region and by diffusing dopant from the third layer into the third doped region.

21. The process of claim 18 wherein the semiconductor material is doped in situ and wherein the material of at least one of the first layer and the third layer comprises doped insulating material, and wherein the process further comprises counterdoping the first doped region with dopant from the first layer and counterdoping the third doped region with dopant from the third layer.

22. The process of claim 21 wherein the step of forming the semiconductor material further comprises:

forming polycrystalline silicon along substantially the entire vertical distance of at least one vertical region of the interior surface of the window; and

melting the polycrystalline silicon to form single-crystalline silicon, and wherein the material of the first and the third layers is doped insulating material, and wherein

during the step of melting, the dopants in the first layer are driven into the adjacent region of the semiconductor material to form the first doped region and dopants in the third layer are driven into the adjacent region of the semiconductor material to form the third doped region.

23. An integrated circuit structure comprising:

a semiconductor substrate having a major surface formed along a plane;

a multi-layer stack overlying the major surface;

a relatively thin first vertical layer of single crystalline material adjacent the vertical surface of a window formed within said multilayer stack, wherein said first layer of single crystalline material comprises a first, a second, and a third doped region, wherein said second doped region is disposed between said first and said third doped regions, and wherein said first and said third doped regions are doped a first conductivity type and said second doped region is doped a second conductivity type;

a dielectric layer adjacent the surface of at least the first and the third doped regions facing the window interior;

an oxide layer adjacent said second doped region; and

a gate over said oxide layer.

24. The integrated circuit structure of claim 23 further comprising a conductive layer adjacent the interior facing surface of the second doped region.

25. The integrated circuit structure of claim 23 further comprising:

a second relatively thin vertical layer of single crystalline material adjacent the vertical surface of the window, wherein said second single crystalline material comprises a fourth, a fifth and a sixth doped region, wherein said fifth doped region is disposed between said fourth and said sixth doped regions, and wherein said fourth and said sixth doped regions are doped a first conductivity type and said fifth doped region is doped a second conductivity type, and wherein said second layer of single crystalline material is formed on an interior surface of the window and insulated from the first vertical layer of single crystalline material also disposed on the interior surface of the window;

a dielectric layer adjacent the surface of at least the fourth and the sixth doped regions facing the window interior;

an oxide layer adjacent said fifth doped region; and

a gate over said oxide layer of said fifth doped region.

26. The integrated circuit structure of claim 23 wherein the first doped region comprises a first source/drain region of a silicon-on-insulator MOSFET, wherein the second doped region comprises a channel region of said silicon-on-insulator MOSFET, and wherein the third doped region comprises a second source/drain region of said silicon-on-insulator MOSFET.

27. An integrated circuit structure comprising:

a semiconductor substrate having a major surface formed along a plane;

a first contact region formed in the surface;

a first insulating layer overlying said first contact region;

a first silicon nitride layer overlying said first insulating layer;

a gate layer overlying said first silicon nitride layer;

a second silicon nitride layer overlying said gate layer;

a second insulating layer overlying said second silicon nitride layer;

a layer of single crystalline material formed along a vertical surface of a window formed within said first insulating layer, said first silicon nitride layer, said gate layer, said second silicon nitride layer, and said second insulating layer, wherein said layer of single crystalline material comprises a first, a second, and a third doped region, wherein said first doped region is adjacent said first insulating layer, and wherein said second doped region is adjacent said gate layer, and wherein said third doped region is adjacent said second insulating layer, and wherein said first and said third doped regions are doped a first conductivity type and said second doped region is doped a second conductivity type;

a layer of insulating material ~~disposed~~ on the inwardly facing surface of at least said first and said third doped regions; and

a gate oxide layer disposed between said gate layer and said second doped region.

28. The integrated circuit structure of claim 27 wherein the first doped region comprises a first source/drain region of an SOI MOSFET, the second doped region comprises a channel region of said SOI MOSFET, and the third doped region comprises a second source/drain region of said SOI MOSFET.

29. The integrated circuit structure of claim 27 further comprising a layer of insulating material disposed on the inwardly facing surface of the second doped region.

30. The integrated circuit structure of claim 27 further comprising a layer of conducting material disposed on the inwardly facing surface of the second doped region.

31. A plurality of silicon-on-insulator transistor structures comprising:

a semiconductor substrate having a major surface formed along a plane;

a first contact region formed in the surface;

a first insulating layer overlying said first contact region;

a silicon nitride layer overlying said first insulating layer;

a gate layer overlying said first silicon nitride layer;

a second silicon nitride layer overlying said gate contact layer;

a second insulating layer overlying said second silicon nitride layer;

a plurality of vertical layers of single crystalline material formed along an interior vertical surface of a window formed within said first insulating layer, said first silicon nitride layer, said gate contact layer, said second silicon nitride layer, and said second insulating layer, wherein each one of said plurality of vertical layers of single crystalline material comprises a first, a second, and a third doped region, and wherein said first and said third doped regions are doped a first conductivity type and said second doped region is doped a second conductivity type;

a layer of insulating material adjacent the inwardly facing surface of at least each one of said first and said third doped regions of said plurality of vertical layers of single crystalline material;

a gate oxide layer disposed between said gate layer and said second doped region of each one of said plurality of vertical layers of single crystalline material;

a plurality of vertical insulating layers interposed between adjacent ones of said plurality of vertical layers of single crystalline material for insulating adjacent ones of said plurality of vertical layers of single crystalline material; and

a conductive region in electrical contact with the inwardly facing surface of said second doped region of each one of said plurality of vertical layers of single crystalline material.

32. The plurality of silicon-on-insulator transistor structures of claim 31 wherein the first doped region of each of the plurality of vertical layers of single crystalline material comprises a source/drain region of an SOI MOSFET, and wherein the second doped region of each one of the plurality of vertical layers of single crystalline material comprises a channel region of said SOI MOSFET, and wherein the third doped region of each one of the plurality of vertical layers of single crystalline materials comprises a second source/drain region of said MOSFET.

33. The plurality of silicon-on-insulator transistor structures of claim 31 further comprising a layer of insulating material adjacent the inwardly facing surface of the second doped region of each one of the plurality of vertical layers of single crystalline materials.

34. The plurality of silicon-on-insulator transistor structures of claim 31 further comprising a layer of conductive material adjacent the inwardly facing surface of the second doped region of each one of the plurality of vertical layers of singly crystalline material.